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Stylesheet Version v1.1.0

**Title of
Invention****A MANUFACTURABLE METHOD AND STRUCTURE FOR DOUBLE
SPACER CMOS WITH OPTIMIZED NFET/PFET PERFORMANCE**

Application Number :

Date :

First Named Applicant: Sadanand V Deshpande

Confirmation Number:

Attorney Docket Number: FIS920030397US1

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Documents being submitted:	Files
us-ids	FIS920030397US1-usidst.xml us-ids.dtd us-ids.xsl
us-request	FIS920030397US1-usrequ.xml us-request.dtd us-request.xsl
us-assignment	FIS920030397US1-usassn.xml us-assignment.xml us-assignment.dtd AFIS920030397US1ass1.tif AFIS920030397US1ass2.tif
us-fee-sheet	FIS920030397US1-usfees.xml us-fee-sheet.xsl us-fee-sheet.dtd
application-body	FIS920030397US1-trans.xml us-application-body.xsl application-body.dtd wipo.ent mathml2.dtd mathml2-qname-1.mod isoamsa.ent isoamsb.ent isoamsc.ent isoamsn.ent isoamso.ent isoamsr.ent isogr3.ent isomfrk.ent isomopf.ent isomscr.ent isotech.ent isobox.ent isocyr1.ent isocyr2.ent isodia.ent isolat1.ent isolat2.ent isonum.ent isopub.ent mmlextra.ent mmlalias.ent soextblx.dtd A20030397dwg1.tif A20030397dwg2.tif A20030397dwg3.tif A20030397dwg4.tif A20030397dwg5.tif
us-declaration	AFIS920030397US1dec1.tif
us-declaration	AFIS920030397US1dec2.tif

Comments

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